

(26) (((bl bitline bit adj line readline read adj line sense adj line
 (2) 6268243.pn.
 (562197) capacitor
 (62) (((bl buried adj (bl bitline bit adj line readline read adj line s
 (9) ("4737829" | "4896293" | "5155059" | "5170243" | "52
 (4) 5840591.URPN
 (3) ("5818745" | "5827092" | "5829228".LPN.
 (4) 5840591.URPN
 (62) (((bl buried adj (bl bitline bit adj line readline read adj line s
 (28) (((bl bitline bit adj line readline read adj line sense adj line
 (74) 5840591.URPN. (((bl buried adj (bl bitline bit adj line read
 (4577) (spacer liner) near9 (oxide near6 nitride)
 (84523) dram
 (152) (spacer liner) near9 (oxide near6 nitride) same dram
 (7551) cap\$4 near9 nitride
 (44) ((spacer liner) near9 (oxide near6 nitride) same dram) and
 (7498) bbl (buried trench \$4) adj bit
 (12) (spacer liner) near9 (oxide near6 nitride) same (bl buried

DB: USPAT:US:POPUB:EPO:JPO:DERWENT:IDM:TOB

Default operator: OR

Plurals
 Highlight all bit terms initially

(((bl buried adj (bl bitline bit adj line readline read adj line sense adj line column)
) and (((bl bitline bit adj line readline read adj line sense adj line column)
) near9 trench) same (((bl bitline bit adj line readline read adj line sense adj line column)
) near9 (etch\$4 trim \$4))) not micron.as.) and capacitor

June 2004

	U	Inventor	Document ID	Issue	P	Title	Current	Current XR	Revised	S	C	P	Image	Doc	P
1	<input type="checkbox"/>	Park, Jae-Kw	US 5840591 A	19981	1	Method of manufacturing buried bit line DR	438/262	257/E21.64		<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 584059	<input type="checkbox"/>
2	<input type="checkbox"/>	Shen, Hua	US 6537870 B1	20030	2	Method of forming an integrated circuit com	438/243	257/E21.65		<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 653787	<input type="checkbox"/>
3	<input type="checkbox"/>	Athavale, Sat	US 6348374 B1	20020	2	Process for 4F2 STC cell having vertical MO	438/243	257/E21.65		<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 634837	<input type="checkbox"/>
4	<input type="checkbox"/>	Lee, Robin et	US 6303424 B1	20011	1	Method for fabricating a buried bit line in a D	438/239	257/E21.65		<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 630342	<input type="checkbox"/>
5	<input type="checkbox"/>	Chen, Min-Lia	US 6271556 B1	20010	1	High density memory structure	257/303	257/301		<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 627155	<input type="checkbox"/>
6	<input type="checkbox"/>	Lee, Tong-Hsi	US 6127228 A	20001	1	Method of forming buried bit line	438/262	257/E21.50		<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 612722	<input type="checkbox"/>
7	<input type="checkbox"/>	Lee, Kang-yo	US 5900659 A	19990	1	Buried bit line DRAM cells	257/296	257/306		<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 590065	<input type="checkbox"/>
8	<input type="checkbox"/>	Beer, Peter	US 20030011010	20030	9	Integrated semiconductor memory and fabric	257/296			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 200300	<input type="checkbox"/>
9	<input type="checkbox"/>	Divakaruni, R	US 20030001200	20030	1	Modified vertical MOSFET and methods of fo	257/330	257/332		<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 200300	<input type="checkbox"/>
10	<input type="checkbox"/>	Asano, Isamu	US 20020155682	20021	6	Method of manufacturing a semiconductor in	438/253	257/E21.64		<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 200201	<input type="checkbox"/>
11	<input type="checkbox"/>	HIEDA, KATS	US 20020153552	20021	2	SEMICONDUCTOR DEVICE AND METHOD FO	257/308	257/E21.00		<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 200201	<input type="checkbox"/>
12	<input type="checkbox"/>	Athavale, Sat	US 20020130346	20020	9	Structure and process for buried bitline and s	257/301	257/E21.65		<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 200201	<input type="checkbox"/>
13	<input type="checkbox"/>	Lee, Thomas	US 20020028541	20020	1	Dense arrays and charge storage devices, an	438/149	257/E27.02		<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 200200	<input type="checkbox"/>
14	<input type="checkbox"/>	Economikos,	US 20010017394	20010	1	Method of forming a buried bitline in a vertic	257/302	257/E21.85		<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 200100	<input type="checkbox"/>
15	<input type="checkbox"/>	Asano, Isamu	US 6696337 B2	20040	6	Method of manufacturing a semiconductor in	438/253	438/241		<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 669633	<input type="checkbox"/>
16	<input type="checkbox"/>	Alsmeyer, Joh	US 6593813 B1	20030	1	Memory cell for plateline sensing	257/308	257/298		<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 659381	<input type="checkbox"/>
17	<input type="checkbox"/>	Athavale, Sat	US 6518118 B2	20030	8	Structure and process for buried bitline and s	438/243	257/E21.65		<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 651811	<input type="checkbox"/>
18	<input type="checkbox"/>	Furukawa, T	US 6440801 B1	20020	7	Structure for folded architecture pillar mem	438/272	257/302		<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 644080	<input type="checkbox"/>